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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/755,990	01/13/2004	Kirk Prall	MIO 0065 VA/40509.282	2259

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EXAMINER	
COLEMAN, WILLIAM D	
ART UNIT	**PAPER NUMBER**
2823	

DATE MAILED: 03/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/755,990	PRALL, KIRK	
	Examiner	Art Unit	
	W. David Coleman	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *01/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statement filed January 13, 2004 fails to comply with 37 CFR 1.98(a)(3) because it does not include a concise explanation of the relevance, as it is presently understood by the individual designated in 37 CFR 1.56(c) most knowledgeable about the content of the information, of each patent listed that is not in the English language. It has been placed in the application file, but the information referred to therein has not been considered.

Specification

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (f) he did not himself invent the subject matter sought to be patented.

4. Claims 1-35 are rejected under 35 U.S.C. 102(b) as being anticipated by Forbes et al., U.S. Patent 5,936,274.

Forbes discloses a semiconductor process as claimed. See FIGS. 1-13 where Forbes teaches the following limitations.

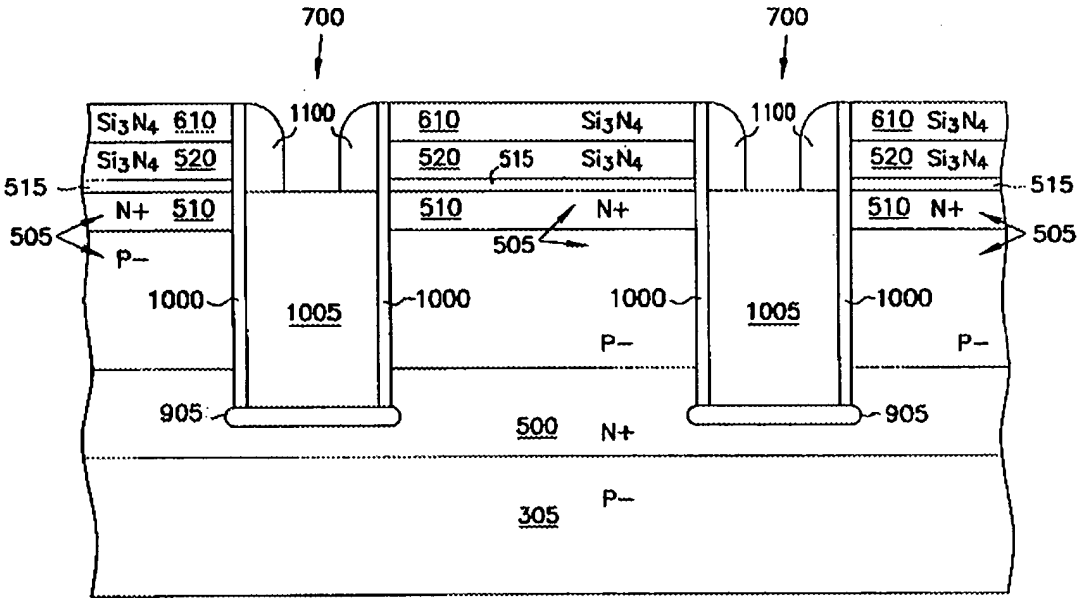

FIG. 11

5. Pertaining to claim 1, Forbes teaches a method of fabricating a memory device comprising:

providing a substrate **305**;

forming a first n-type layer over the substrate **500**;

forming a p-type layer over the first n-type layer **505**;

forming a second n-type layer **510** over the p-type layer;

forming a floating gate over the substrate **325**;

etching a trench in the p-type layer of said memory device; and

forming a select gate in the trench, wherein said memory device defines a square feature size of $2F^2$.

6. Pertaining to claim 2, Forbes teaches the method of claim 1, wherein forming a first n-type layer over the substrate comprises forming a buried source over the substrate **500**.

7. Pertaining to claim 3, Forbes teaches the method of claim 1, wherein forming a first p-type layer over the first n-type layer comprises forming a first p-type layer over the first n-type layer using epitaxial deposition.

8. Pertaining to claim 4, Forbes teaches the method of claim 1, forming a p-type layer over the first n-type layer comprises forming a vertical channel over the first n-type layer.

9. Pertaining to claim 5, Forbes teaches a method of fabricating a buried source comprising: providing a wafer having a substrate;

covering a periphery of a wafer using an array mask;

doping source areas with a dopant; and

performing an epitaxial deposition to form a p-type channel, wherein performing an epitaxial deposition to form a p-type channel comprises performing an epitaxial deposition to form a p-type channel to a determined thickness, wherein the thickness determines a channel length.

10. Pertaining to claim 6, Forbes teaches the method of claim 5, wherein doping source areas with a dopant comprises doping source areas with As (please see the various references cited which are incorporated by reference).

11. Pertaining to claim 7, Forbes teaches the method of claim 5, wherein doping source areas with a dopant comprises doping source areas with Sb (in particular, see Gonzalez, U.S. Patent 5,640,342).

12. Pertaining to claim 8, Forbes teaches a method of fabricating a memory device comprising:

providing a wafer having a substrate;

forming a buried source in the substrate; forming a vertical channel over the buried source;

performing a cell implant; forming a tunnel oxide layer over the substrate; forming a first poly layer over the tunnel oxide layer;

forming a nitride layer over the first poly layer; patterning wordlines into the memory device, wherein the memory device defines a square feature size of less than 4F2;

forming STI areas in the memory device;

removing the nitride layer; and forming an oxide nitride oxide layer over a surface of the memory device.

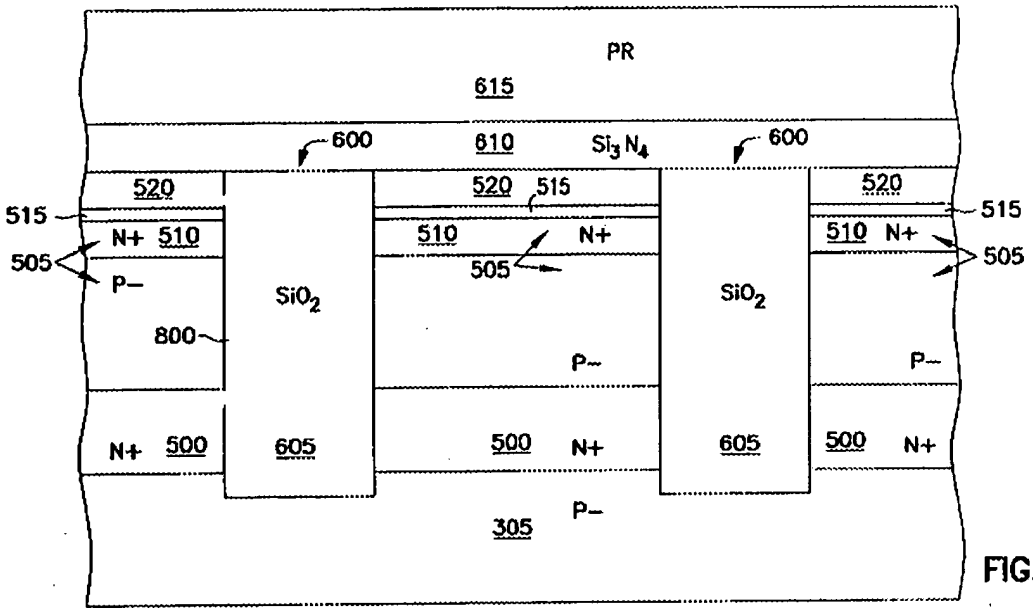

FIG. 6

13. Pertaining to claim 9, Forbes teaches the method of claim 8, wherein forming STI areas in the memory device further comprises etching the nitride layer and etching the first poly layer.

14. Pertaining to claim 10, Forbes teaches the method of claim 8, wherein forming STI areas in the memory device further comprises depositing a STI oxide over the STI areas and filling the STI areas with a field oxide.

15. Pertaining to claim 11, Forbes teaches the method of claim 8, further comprising: polishing a surface of the memory device using chemical mechanical polishing to make the surface planar (column 9, line 44).

16. Pertaining to claim 12, Forbes teaches a method of fabricating a memory device comprising:

providing a wafer having a substrate;

forming a buried source over the substrate;

forming a vertical channel over the buried source; forming a STI area and a self aligned floating gate;

depositing a BPSG layer over the substrate; depositing a hardmask layer over the BPSG layer;

patterning active areas to form an active trench;

forming first spacers along sidewalk of the active trench; forming a drain in the active trench; and

forming a wordline over the drain, wherein said memory device defines a square feature size of less than 4F2.

17. Pertaining to claim 13, Forbes teaches the method of claim 12, further comprising performing RTP on the memory device and

polishing the surface of the memory device prior to depositing a hardmask layer.

18. Pertaining to claim 14, Forbes teaches the method of claim 12, wherein patterning active areas further comprises etching through the hardmask layer, the BPSG layer, an oxide nitride oxide layer and a first poly layer.

Pertaining to claim 15, Forbes teaches the method of claim 12, wherein forming first spacers comprises depositing a first spacer layer and etching the first spacer layer thereby leaving the first spacers along the sidewalls of the active trench.

19. Pertaining to claim 16, Forbes teaches the method of claim 12, further comprising: forming a TiN layer over the active trench; and forming a TiSi layer over the active trench.

20. Pertaining to claim 17, Forbes teaches the method of claim 12 further comprising: performing a RTP on the memory device prior to forming a wordline.

21. Pertaining to claim 18, Forbes teaches the method of claim 12, wherein forming a wordline comprises: depositing a wordline layer over the active trench; polishing the wordline layer such that the wordline layer is planar to the hardmask layer; and removing a portion of the wordline layer such that a lower portion of the wordline layer remains.

22. Pertaining to claim 19, Forbes teaches the method of claim 18, wherein removing a portion of the wordline layer comprises removing substantially half of the wordline layer.

Pertaining to claim 20, Forbes teaches the method of claim 12, further comprising depositing a second spacers over the wordline.

23. Pertaining to claim 21, Forbes teaches a method of fabricating a memory device comprising: forming active areas in a substrate;

forming a floating gate layer over the substrate;

patterning rowlines in the memory device;

forming a removable. spacer over the Towlines; and etching a select trench in the substrate, wherein the memory cell defines a square feature size of about $2F^2$.

24. Pertaining to claim 22, Forbes teaches the method of claim 21 further comprising: removing the removable spacer;

forming a select transistor oxide layer over the select trench;

forming a second poly layer over the surface of the memory device;

forming a conductive layer over the second poly layer; and patterning the second poly layer and the conductive layer.

25. Pertaining to claim 23, Forbes teaches the method of claim 22, wherein forming a conductive layer over the second layer comprises forming a WSi, layer over the second poly layer (see Doan, U.S. Patent 5,223,081 which is incorporated by reference).

26. Pertaining to claim 24, Forbes teaches the method of claim 22, wherein forming a second poly layer over the surface of the memory device further comprises forming the second poly layer in the select trench to form a select gate.

27. Pertaining to claim 25, Forbes teaches a method of forming a memory device comprising: forming a buried source formed in a substrate;

forming a first layer over said substrate;

forming a first drain formed in said first layer so as to define a first substantially vertical channel between said first drain and said buried source;

forming a trench in said first layer;

forming a select gate in said trench; and

forming a horizontal first floating gate over said first layer adjacent to said trench and proximate to said first substantially vertical channel, wherein said first floating gate is dimensioned so as to define a sublithographic gate and the square feature size of the memory cell is not greater than $2F^2$.

28. Pertaining to claim 26, Forbes teaches the method of forming a memory device according to claim 25, further comprising:

forming a second drain formed in the first layer so as to define a second substantially vertical channel between said second drain and said buried source; and

forming a second floating gate over the first layer adjacent to the trench and proximate to the second substantially vertical channel.

29. Pertaining to claim 27, Forbes teaches the method of forming a memory device according to claim 25, wherein the floating gate is formed such that at least a portion of the floating gate overlies at least a portion of the drain.

30. Pertaining to claim 28, Forbes teaches the method of forming a memory device according to claim 25, wherein said trench is formed such that it extends through the first layer to the buried source.

31. Pertaining to claim 29, Forbes teaches the method of claim 25, wherein said formation of said source comprises forming a n-type layer over a substrate.

32. Pertaining to claim 30, Forbes teaches the method of claim 25, wherein said formation of said drain comprises forming a n-type layer over the source.

33. Pertaining to claim 31, Forbes teaches the method of claim 25, wherein said formation of said floating gate layer comprises: forming a tunnel oxide layer; forming a polysilicon layer over the tunnel oxide layer; and forming an oxide layer over the polysilicon layer.

34. Pertaining to claim 32, Forbes teaches the method of claim 25, wherein said formation of said select gate comprises: forming an oxide layer in the select trench; and filling the select trench with polysilicon.

35. Pertaining to claim 33, Forbes teaches a method of forming a memory device comprising:

forming a first layer defining a source;

forming a second layer over the first layer;

forming a drain in the second layer so as to define a substantially vertical channel between said source and said drain; forming a trench in the second layer;

forming a select gate in the trench; and

forming a horizontal floating gate over the second layer adjacent to the trench so as to avoid extending vertically down into the trench below the second layer, wherein the floating gate is dimensioned so as to define a sublithographic gate and the square feature size of the memory cell is not greater than $2F^2$.

36. Pertaining to claim 34, Forbes teaches the method of forming a memory device according to claim 33, wherein the trench is formed so as to extend through the second layer and into the first layer.

37. Pertaining to claim 35, Forbes teaches a computer system comprising at least one processor, a system bus, and a memory device

coupled to the system bus, the memory device including at least one memory cell comprising:

a source;

a substantially vertical channel formed over the source;

a drain formed over the vertical channel; and

a substantially horizontal floating gate formed over at least a portion of the drain, wherein the square feature size of the memory cell is not greater than $2F^2$.

Conclusion

38. Any inquiry concerning this communication or earlier communications from the examiner should be directed to W. David Coleman whose telephone number is 571-272-1856. The examiner can normally be reached on Monday-Friday 9:00 AM-5:30 PM.

39. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 571-272-1855. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

40. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

W. David Coleman
Primary Examiner
Art Unit 2823

WDC